

# EN0-001<sup>Q&As</sup>

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**QUESTION 1**

When an ARMv7-A MPCore system is in SMP mode, which of the following TWO operations can the processor handle automatically? (Choose two)

- A. Coherency management between all L1 data caches
- B. Broadcast of some inner-shared cache and TLB maintenance operations
- C. Broadcast of some outer-shared cache and TLB maintenance operations
- D. Coherency management between all L1 instruction caches
- E. Coherency management between all external caches

Correct Answer: AB

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**QUESTION 2**

What type of instruction is used for cache maintenance operations?

- A. Dedicated ARM instructions
- B. Dedicated Thumb instructions
- C. CP14 instructions
- D. CP15 instructions

Correct Answer: D

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**QUESTION 3**

Which of the following best describes the relationship between Tightly Coupled Memories (TCM), Level 1 (L1) and Level 2 (L2) cache memory systems?

- A. TCMs are a part of only L1 cache system
- B. TCMs are a part of only L2 cache system
- C. TCMs are part of both L1 and L2 cache systems
- D. TCMs are not part of either L1 or L2 cache systems

Correct Answer: D

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**QUESTION 4**

Which one of the following features must any processor support to conform to the ARMv7-A architecture?

- A. NEON (Advanced SIMD)
- B. Thumb-2 technology
- C. TrustZone (Security Extensions)
- D. Generic Interrupt Controller

Correct Answer: B

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#### QUESTION 5

Which of these C99 keywords can be used to indicate that two arrays do not overlap?

- A. "pure"
- B. "volatile"
- C. "static"
- D. "restrict"

Correct Answer: D

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